CLAIMS

Having described the invention, what is claimed is:

1. A method for processing a request, comprising the steps of: determining whether the request is speculative or not based upon a first identifier; assessing one or both of interconnect and target resource conditions in the event that the request is speculative; and either processing the request, or not, as a function of the conditions.

2. The method of claim 1, wherein the step of determining whether the request is speculative comprises decoding first identifier as a first bit field within the request.

3. The method of claim 2, further comprising encoding the first bit field within the request to define a speculative ID of the request.

4. The method of claim 1, wherein the request comprises one of an instruction, message and operational request.

5. The method of claim 1, further comprising the step of determining a priority of the request based upon a second identifier, in the event that the request is speculative, and wherein the step of processing the request comprises processing the request, or not, based upon the conditions and the priority.

6. The method of claim 5, wherein the step of determining a priority comprises decoding the second identifier as a second bit field within the request.

7. The method of claim 6, further comprising encoding the second bit field within the request to define a priority of the request.

8. The method of claim 1, wherein the request comprises one of a memory read request and a memory load request.

9. The method of claim 1, wherein the step of determining comprises utilizing one of a CPU, chipset and memory controller to determine whether the request is speculative.

10. The method of claim 9, wherein at least one of the CPU, chipset and memory controller independently controls the step of processing the request based on the conditions.

11. The method of claim 1, wherein the step of assessing target resource conditions comprises assessing one or more of memory utilization, memory congestion, buffer space utilization, and bus congestion.

12. The method of claim 1, wherein the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization.

13. The method of claim 1, further comprising the step of notifying one or more logic devices when the request is not processed.

14. In CPU architecture of the type that initiates both speculative and non-speculative memory requests, the improvement comprising decode logic for determining whether the requests are speculative, and assessment logic for determining one or both of interconnect and target resource conditions, the CPU architecture processing speculative requests, or not, as a function of the conditions.

15. In CPU architecture of claim 14, the further improvement comprising a prefetch unit for prefetching speculative requests, wherein the decode logic detects whether prefetched requests are speculative.

16. A system for processing speculative requests, comprising: one or more requests having a bit field defining the requests as speculative or non-speculative; decode logic for decoding the bit field to determine whether one or more requests are speculative; and processing logic for processing speculative requests, or not, based on at least one of interconnect and target resource conditions.

17. A system of claim 16, one or both of the decode logic and processing logic being selected from the group consisting essentially of a CPU, a chipset, a bus controller and a memory controller.

18. A system of claim 16, wherein the requests comprise memory read instructions.

19. A system of claim 16, further comprising a bus controller for assessing one or more of bus congestion and bus utilization conditions.